1. (Amended) A host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising:

a processor;

a host memory coupled to said processor; and

a host-fabric adapter coupled to said processor and provided to interface with said switched fabric, including an internal cache to store selected translation and protection table (TPT) entries from said host memory for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, a translation cacheable flag to specify whether said host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory;

wherein said host-fabric adapter is configured to flush individual cached translation and protection table (TPT) entry from said internal cache in accordance with the corresponding translation cacheable flag.

3. (Amended) The host as claimed in claim 1, wherein each of said selected translation and protection table (TPT) entries represents translation of a single page of said host memory.

4. (Amended) The host as claimed in claim 1, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected translation and protection table (TPT) entries.

6. (Amended) The host as claimed in claim 1, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.

7. (Amended) The host as claimed in claim 1, wherein said host-fabric adapter flushes a designated cached translation and protection table (TPT) entry from said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a first logic state, and maintains said designated cached translation and protection table (TPT) entry in said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a second logic state opposite of said first logic state.

9. (Amended) A network, comprising:

a switched fabric;

I/O controllers attached to said switched fabric; and

a host comprising an operating system, a host memory, and a host-fabric adapter including translation and protection table (TPT) entries , each TPT entry comprising protection attributes to control read and write access to a given memory region of the host memory, a translation cacheable flag to specify whether the host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether the host-fabric adapter has permission to access the host memory,

wherein the host-fabric adapter is configured to cache selected TPT entries from the host memory and to flush individual cached translation and protection table (TPT) entry in accordance with the corresponding translation cacheable flag.

14. (Amended) The network as claimed in claim 9, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.